UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/459,703	12/13/1999	Kiran A. Padwekar	884.027US1	1539

21186 7590 08/14/2002

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
MEONSKE, TONIA L	
ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 08/14/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	**Application No.** 09/459,703	**Applicant(s)** PADWEKAR, KIRAN A.	
	Examiner Tonia L Meonske	**Art Unit** 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 April 2001* .

2a)□ This action is **FINAL**. 2b)☒ This action is non-final.

3)□ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)□ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☒ Claim(s) *3 and 4* is/are objected to.

8)□ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 December 1999* is/are: a)□ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)□ The proposed drawing correction filed on _____ is: a)□ approved b)□ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)□ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)□ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)□ All b)□ Some * c)□ None of:

1.□ Certified copies of the priority documents have been received.

2.□ Certified copies of the priority documents have been received in Application No. _____ .

3.□ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)□ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) □ The translation of the foreign language provisional application has been received.

15)□ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) □ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) □ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .

4) □ Interview Summary (PTO-413) Paper No(s). _____ .

5) □ Notice of Informal Patent Application (PTO-152)

6) □ Other: .

DETAILED ACTION

Drawings

1.) The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: "404" on page 4, line 20, "120" on page 15, line 7. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2.) The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: "200" in Figure 2. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3.) The drawings are objected to because on page 15, line 5, the applicant refers to a plurality of processors as element "410", please refer to the plurality of processors as "410(1)-410(n)", which is consistent with the drawings. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

4.) The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

5.) Claims 3 and 4 are objected to because of the following informalities: On page 17, claim 3, line 1, "the the" should read "the"; On page 17, claim 4, line 1, "on" should read "one". Appropriate correction is required.

Claim Rejections - 35 USC § 103

6.) The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7.) Claims 1-4 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mealey et al, US Patent 5,963,737 in view of Zumkehr et al., US Patent 6,247,118 B1.

8.) Referring to claims 1 and 2, Mealey et al. have taught a system comprising:

(a.) a storage element (Figure 1, element 12, Main Memory);

(b.) a memory hierarchy (Instruction Cache) coupled to the storage element (on page 3, line 36, a cache miss exception is mentioned, so an instruction cache connected to the main memory is inherently present);

(c.) a processor coupled to the memory hierarchy (Instruction Cache) (Figure 1, element 11, the instruction cache is inherently coupled to the processor),

9.) But he does not specifically teach wherein the processor executes instructions from the memory hierarchy and a replay handler is loaded into the memory hierarchy and the processor executes the replay handler for replaying at least one execution. (column 4, lines 27-45, the exception handler is the handler for playing at least one execution by processing the exception, the exception handler is inherently loaded into the instruction cache) However it is obvious that the exception that is detected could be an error of a previous instruction, whereby instructions would need to be reexecuted in order to recover from the exception, or error, as taught by Zumkehr et al. (column 5, lines 50-61) It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the exception handler taught by Mealey et al. be the replay handler as taught by Zumkehr et al. for the desirable purpose of being able to recover from an error.

10.) Referring to claim 3, Mealey et al have taught the system of claim 1 wherein the replay handler is loaded into the memory hierarchy in response to a signal. (column 4, lines 27-45, an exception to load the replay handler into the instruction cache is signaled by the hardware)

11.) Referring to claim 4, Mealey et al. have taught the system of claim 1 wherein the replay handler includes the at least one execution. (column 4, lines 27-45, there is at least one execution when the exception is processed in the first-level interrupt handler)

12.) Referring to claim 17, Mealey et al. have taught a method for replaying executions comprising:

(a.)interrupting normal processor execution; (Figure 6, an exception is signaled(element 50) and normal processor execution is interrupted)

(b.)loading a replay/restart kernel; (abstract, column 4, lines 27-54 the first and second level interrupt handlers are part of the kernel and they are inherently loaded into an instruction cache for executing the exception) (c.) playing at least one execution; (Figure 6, column 4, lines 27-45, the exception handler plays at least one execution by processing the exception) and (d.)resuming normal executions. (Figure 6, the state is restored (element 68) and the processor returns to normal execution (element 69))

13.) Mealey et al. has not specifically taught replaying at least one execution. However it is obvious that the reason for interrupting normal processor execution is because an error of a previous instruction is detected, whereby instructions would need to be reexecuted in order to recover from the exception, or error, as taught by Zumkehr et al. (column 5, lines 50-61) It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the exception handler taught by Mealey et al. be the replay handler as taught by Zumkehr et al. for the desirable purpose of being able to recover from an error.

14.) Referring to claim 18, Mealey et al. have taught the method of claim 17, as described above, further comprising generating the at least one execution. (column 4, lines 27-45, there is at least one execution that is generated when the exception is processed in the first-level interrupt handler)

15.) Referring to claim 19, Mealey et al. have taught the method of claim 18, as described above, further comprising accessing state information. (Figure 6, state information is accessed in elements 57, 68, 60 and 60a)

16.) Claims 5, 10, and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mealey et al., US Patent 5,963,737 in view of Argade et al., US Patent 5,724,505 and further in view of Zumkehr et al., US Patent 6,247,118 B1.

17.) Referring to claim 5, Mealey et al. have taught the system of claim 1 wherein the replay handler loads the at least one execution into the memory hierarchy but he didn't specifically teach that it was from an external device. However, Argade et al. have taught an external debug host computer (column 4, lines 39-65) that sends at least one signal or execution in an analogous art for the purpose of debugging. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the atleast one execution, as taught by Mealey et al., come from an external device, as taught by Argade et al. for the desirable purpose of debugging the system.

18.) Referring to claim 10, Mealey et al. have taught a system comprising:

(a.) a memory hierarchy; (on page 3, line 36, a cache miss exception is mentioned, so an instruction cache, or memory hierarchy, connected to the main memory is inherently present)

(b.) a processor coupled to the memory hierarchy (Figure 1, element 11, the instruction cache is inherently coupled to the processor) wherein the processor executes instructions from the memory hierarchy; (the processor inherently executes instructions from the instruction cache)

(c.) a port coupled to the processor and memory hierarchy; (there is inherently a port coupled to the processor and instruction cache in order to transfer data from the instruction cache to the processor to be executed)

(d.) the system generates a handler, generates at least one execution and generates a signal for playing the at least one execution. (column 4, lines 27-45, the exception handler is the handler for playing at least one execution by processing the exception, the exception handler is inherently loaded into the instruction cache, an exception to load the handler into the instruction cache is signaled by the hardware)

19.) Mealey et al. have not specifically taught that the handler is a replay handler for replaying at least on execution. However it is obvious that the exception that is detected could be an error of a previous instruction, whereby instructions would need to be reexecuted in order to recover from the exception, or error, as taught by Zumkehr et al. (column 5, lines 50-61) It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the exception handler taught by Mealey et al. be the replay handler as taught by Zumkehr et al. for the desirable purpose of being able to recover from an error.

20.) Mealey et al. also have not specifically taught a host system coupled to the port; wherein the host system generates the replay handler, generates the least one execution and generates the signal for replaying the at least one execution.

21.) However, Argade et al. have taught an external debug host computer with a port coupled to the processor (column 4, lines 39-65) that sends at least one signal or execution in an analogous art for the purpose of debugging, or replaying instructions. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the atleast one execution, as taught by Mealey et al., come from an external host system, as taught by Argade et al. for the desirable purpose of debugging the system.

22.) Referring to claim 14, Mealey et al. and Argade et al. have taught the system of claim 10, as described above, and wherein a replay state is sent to the host system through the port. (Argade et al.;Column 4, lines 39-65, the program is traced, so values must inherently be passed back to the debug host computer through the port, element 44)

23.) Referring to claim 15, Mealey et al. and Argade et al. have taught the system of claim 10, wherein the port is a network interface. (the host debug computer (100) is connected, or networked to the digital microprocessor in Argade et al., so the port (44) is a network interface for debugging purposes)

24.) Referring to claim 16, Mealey et al. and Argade et al. have taught the system of claim 10, wherein the port is a serial interface.(Argade et al. column 3, lines 34-36)

25.) Claims 6-9, and 20-22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mealey et al., US Patent 5,963,737 in view of Edgington et al., US Patent 5,530,804 and further in view of Zumkehr et al., US Patent 6,247,118 B1.

26.) Referring to claim 6, Mealey et al. have taught a system for replaying executions comprising:

(a.) a storage element; (Figure 1, element 12, Main Memory)

(b.) a memory hierarchy coupled to the storage element; (on page 3, line 36, a cache miss exception is mentioned, so an instruction cache, or a memory hierarchy, connected to the main memory is inherently present)

(c.) a system bus coupled to the memory hierarchy; (Figure 1, element 15) (d.)a processor coupled to the system bus (Figure 1, element 11), wherein the processor executes instructions from the memory hierarchy and wherein on a break, the processor reaches a steady state, loads a handler into the memory hierarchy and the processor executes the handler to play at least one execution. (Figure 6, when an exception, or break, is signaled the state is saved in the main memory (element 57), column 4, lines 27-45, the exception handler is the handler for playing at least one execution by processing the exception)

27.) Mealey et al. have not taught that the handler is specifically a replay handler for replaying instructions. However it is obvious that the exception or break that is detected could be an error of a previous instruction, whereby instructions would need to be reexecuted in order to recover from the exception, or error, as taught by Zumkehr et al. (column 5, lines 50-61) It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the exception handler taught by Mealey et al. be the replay handler as taught by Zumkehr et al. for the desirable purpose of being able to recover from an error.

28.) Mealey et al. have also not taught wherein the processor transfers original code of the memory hierarchy to the storage element. However Edgington et al. have taught transferring original code of he instruction cache to a storage element. (Column 13, lines 54-column 14, line 4) so that normal mode can be fully restored after testing and debugging is complete with no adverse changes. It would have been obvious to one of ordinary skill in that art at the time the invention was made to have the system as taught by Mealey et al. transfer the original code of the instruction cache to a storage element, as taught by Edmington et al. in order to fully restore the system after testing, debugging, or any other exception.

29.) Referring to claim 7, Mealey et al. have taught the system of claim 6, as described above, but they have not specifically taught wherein the original code is loaded into the memory hierarchy after the at least one execution has been replayed. However, Edgington et al. have taught wherein the original code is reloaded after debugging the system in order to restore the system to the normal mode of operation (Column 13, line 54-column 14, line 4) It would have been obvious to one of ordinary skill in that art at the time the invention was made to have the system as taught by Mealey et al. load the original code back into the instruction cache, as taught by Edmington et al. in order to fully restore the system after testing, debugging, or any other exception.

30.) Referring to claim 8, Mealey et al. have taught the system of claim 6, as described above, further comprising a system memory and wherein the storage element is a location in the system memory. (Figure 1, element 12, Main Memory is the system memory)

31.) Referring to claim 9, Mealey et al. have taught the system of claim 6, as described above, but they have not specifically taught wherein the storage element in a hard drive. However, having the storage element be a hard drive allows for a greater capacity for state information to be stored and the information would be non-volatile, so the information would not be lost in the absence of power. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the system, as taught by Mealey et al., have the storage element be a hard drive so that a greater amount of state information could be stored and the information would not be lost when power is absent.

32.) Referring to claim 20, Mealey et al. have taught a method comprising:

(a.) interrupting processes executing on a processor; (Figure 6, an exception is signaled (element 50) and normal processor execution is interrupted)

(b.) storing minimal state information sufficient to later resume the interrupted processes; (Figure 6, elements 60, 60a, and 57)

(c.) loading a replay handler into the instruction cache; (column 4, lines 27-45, the exception handler is the replay handler for playing at least one execution by processing the exception, the exception handler is inherently loaded into the instruction cache)

(d.)branching execution of the processor to the replay handler; (Figure 6, elements 61, 62, and 67)

(e.) playing a system execution a number of times from a starting point to a stopping point while monitoring state information; (column 4, lines 27-45, column 8, lines 7-40, the performance monitor monitors state information while playing a system execution, exception, or interrupt)

(f.) resuming interrupted processes utilizing the minimal state information. (Figure 6, the state is restored (element 68) and the processor returns to normal execution (element 69))

33.) Mealey et al. have not specifically taught replaying a system execution. However it is obvious that the exception or interupt that is detected could be an error of a previous instruction, whereby instructions would need to be reexecuted in order to recover from the exception, or error, as taught by Zumkehr et al. (column 5, lines 50-61) It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the exception handler taught by Mealey et al. be the replay handler as taught by Zumkehr et al. for the desirable purpose of being able to recover from an error.

34.) Mealey et al. have not specifically taught storing original code of an instruction cache and loading the original code into the instruction cache. However Edgington et al. have taught transferring original code of he instruction cache to a storage element. (Column 13, lines 54-column 14, line 4) so that normal mode can be quickly and fully restored after testing and debugging is complete with no adverse changes. It would have been obvious to one of ordinary skill in that art at the time the invention was made to have the system as taught by Mealey et al. sotring the original code of the instruction cache and loading the original code into the instruction cache, as taught by Edmington et al. in order to quickly and fully restore the system after testing, debugging, or any other exception.

35.) Referring to claim 21, Mealey et al. and Edgington et al. have taught the method of claim 20, as described above, but they have not specifically taught modifying the number of times, the starting point and the stopping point by a user. However if there is a test being run, a user must be performing the test. The user would want to be able to control every aspect of the test including the number of times and the starting and stopping points of the test so the user could extract desired information. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the system as taught by Mealey et al. to have the user modify the number of times and the starting and stopping point in order to extract desired information.

36.) Referring to claim 22, Mealey et al. have taught the method of claim 20, as described above, further comprising generating the system execution by tracing an execution of a program. (Column column 2, lines 24-45, the program is traced for an exception and the state is saved and the address location is checked to see if an exception has been registered, and if so the address is used to go to the first-level exception handler)

37.) Claims 11-13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mealey et al., US Patent 5,963,737 in view of Edgington et al., US Patent 5,530,804 and further in view of Zumkehr et al., US Patent 6,247,118 B1, and further in view of Edgington et al., US Patent 5,530,804.

38.) Referring to claim 11, Mealey et al. and Argade et al. have taught the system of claim 10, as described above, wherein the replay handler is loaded into the memory hierarchy from the host system through the port (the exception handler is inherently loaded into the instruction cache through the port), and the replay handler is executed by the processor (column 4, lines 27-45) Mealey et al. have not specifically taught wherein on the signal, original code of the memory hierarchy is saved. However Edgington et al. have taught transferring original code of the instruction cache to a storage element. (Column 13, lines 54-column 14, line 4) so that normal mode can be fully restored after testing and debugging is complete with no adverse changes. It would have been obvious to one of ordinary skill in that art at the time the invention was made to have the system as taught by Mealey et al. save original code of the memory hierarchy, as taught by

Edmington et al. in order to fully restore the system after testing, debugging, or any other exception.

39.) Referring to claim 12, Mealey et al., Argade et al., and Edgington et al. have taught the system of claim 11, as described above, but they have not specifically taught wherein on the replay handler being executed, the replay handler is modifiable by the host system. However when there is a test being run, a user must be performing the test. The user would want to be able to control every aspect of the test including modifying the test so the user could extract desired information. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the system as taught by Mealey et al. to have the user modify the replay handler in order to extract desired information.

40.) Referring to claim 13, Mealey et al., Argade et al., Edgington et al. have taught the system of claim 12, as described above, but they have not taught wherein the replay handler is modified to alter starting and stopping points of one of the at least one executions. However if there is a test being run, a user must be performing the test through the host port. The user would want to be able to control every aspect of the test including the starting and stopping points of one of the atleast executions so the user could extract desired information. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the system as taught by Mealey et al. to have the user modify the starting and stopping point in order to extract desired information.

41.) Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mealey et al., US Patent 5,963,737 and further in view of Zumkehr et al., US Patent 6,247,118 B1.

42.) Referring to claim 23, Mealey et al. have taught computer instructions for

(a.)instructing a processor to perform a method of generating at least one execution; (column 4, lines 27-45, there is at least one execution generated when the exception is processed in the first-level interrupt handler or in the second-level interrupt handler)

(b.)interrupting normal processing; (Figure 6, an exception is signaled (element 50) and normal processor execution is interrupted)

(c.)loading a handler; playing at least one execution; (column 4, lines 27-45, the exception handler is the handler for playing at least one execution by processing the exception, the exception handler is inherently loaded into the instruction cache)

43.) Mealey et al. have not specifically taught that the handler is a replay handler for replaying at least one execution. However it is obvious that the reason that the program is interrupted is because an error of a previous instruction is detected, whereby instructions would need to be reexecuted in order to recover from the exception, or error, as taught by Zumkehr et al. (column 5, lines 50-61) It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the exception handler taught by Mealey et al. be the replay handler as taught by Zumkehr et al. for the desirable purpose of being able to recover from an error.

44.) Mealey et al. has also taught:

(a.) accessing state information; (Figure 6, elements 60, 60a, 57, and 68)

(b.) storing state information; (Figure 6, element 57) and

(c.) resuming normal processing. (Figure 6, element 69)

45.) Mealey et al. have not specifically taught that these instructions are contained on a computer readable medium. However it is known that instructions are usually stored on a computer readable medium to allow a computer to execute the instructions. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the instructions contained on a computer readable medium as it is known that instructions being stored on a computer readable medium allow the instructions to be executed.

Conclusion

46.) The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

(a.) Akkaray, US Patent 6,240,509 B1, has taught and out-of-pipeline trce buffer for holding instructions that may be re-executed following misspeculation.

(b.) Zumkehr et al., US Patent 6,247,118 B1, have taught systems and methods for transient error recovery in reduced instruction set computer processors via instruction retry.

(c.) Jaggar et al., US Patent 6,343,358 B1, have taught executin multiple debug instructions.

(d.)Croquette et al., US Patent 6,311,292 B1, have taught a circuit architecture and method for analyzing the operation of a digital processing system.

47.) Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (703) 305-3993. The examiner can normally be reached on Monday-Friday, 8-4:30.

48.) If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

49.) Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

tlm
August 12, 2002

Eddie Chan

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100